

AKIMA-DTSV 25 MAR 2005 MORRISON & FOERSTER LLP

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From: Robert E. Scheid - Reg. No. 42,126

Date:

March 24, 2005

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Re: U.S. Application No. 10/618,237 filed July 11, 2003

For: ANALOG INTEGRATED CIRCUIT LAYOUT DESIGN

By: Gang ZHANG et al. Examiner: Not Yet Assigned

Group Art Unit: 2825

Our Reference: 18812-2003300

Attached are the following:

- 1. Transmittal (1 page)
- 2. Request for Corrected Filing Receipt (2 pages)
- 3. Copy of Filing Receipt with indicated corrections (2 pages)
- 4. Application Data Sheet (3 pages)

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Winds that Charles	soria ale requies io les	Application Number		10/618,237				
TRANSMITTAL			Filing Date		July 11, 2003			
FORM			First Named Inventor		Gang ZHANG			
(to be used for all correspondence after initial filling)			Art Unit		2825			
•			Examiner Name		Not Yet Assigned			
Total Number of Pages in This Submission		sion 8	Attorney Docket Number		188122003300			
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Fee Transi	mittal Form	Drawing(s)	٠.		After Allowance Communication to TC			
Fee Attached		Licensing-related Papers			Appeal Communication to Soard o Appeals and Interferences			
Amendme	nt/Reply	Petition			Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)			
After	Final	Petition to Convert to a Provisional Application			Proprietary Information			
Affid	avits/declaration(s)	Power of Attorney, Revocation Change of Correspondence Address			Status Letter			
Extension	of Time Request	Terminal Disclaimer			Other Enclosure(s) (please identify below):			
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Certified Copy of Priority Document(s)				P	. Application Data Sheet (3 ages)			
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	Application y to Missing Parts under							
	FR 1.52 or 1.53							
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Firm Name MORRISON & FOERSTER LLP (Customer No. 20872)								
Signature	Dehora	/						
Printed name	Robert E. Scheid	-	A.A.A.					
Date	March 24, 2005		Reg. No.	4	2,126			
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I hereby certify to 9195, on the dat	hat this correspondence is b to shown below.	//	1/	dem	ark Office, facsimile no. (703) 748-			
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Dated: March 24, 2005

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Docket No.: 188122003300

(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Gang ZHANG et al.

Application No.: 10/618,237

Filed: July 11, 2003

Art Unit: 2825

For: ANALOG INTEGRATED CIRCUIT LAYOUT

DESIGN

Examiner: Not Yet Assigned

REQUEST FOR CORRECTED FILING RECEIPT

Filing Receipt Corrections
Office of Initial Patent Examination
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant hereby requests that a corrected Filing Receipt be issued in the aboveidentified patent application. The official Filing Receipt received by Applicant, a copy of which is attached hereto, has the following errors:

Under ATTY DOCKET NO, please delete "2879-030687" and replace with -188122003300-.

Under ADDRESS, please delete "28289 Webb Zieshenheim Logsdon Orkin & Hanson, P.C. 700 Koppers Building 436 Seventh Avenue Pittsburgh, PA 15219" and replace with -20872 Morrison & Foerster LLP 425 Market Street San Francisco, CA 94105-.

Applicants enclose an Application Data Sheet, which reflects corrected attorney docket number and customer number. The Commissioner is hereby authorized to charge any additional

sf-1889468

Application No.: 10/618,237

2

Docket No.: 188122003300

fees under 37 C.F.R. § § 1.16 and 1.17 that may be required by this petition or to credit any overpayment to Deposit Account No. 03-1952 referencing docket no. 188122003300.

Applicant additionally requests that all pertinent U.S. Patent and Trademark Office records relating to the subject application be changed to reflect this correction.

Dated: March 24, 2005

Respectfully submitted,

Robert E. Scheid

Registration No.: 42,126

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San Francisco, California 94105-2482

(415) 268-6369



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APPL NO.	FILING OR 371 (c) DATE	ARTUNIT	FIL FEE REC'D	ATTY.DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/618,237	07/11/2003	2825	375 -	2879-030687-	6	14	3

CONFIRMATION NO. 4647

28289 - WEBB ZIESENHEIM LOGSDON ORKIN & HANSON, P.C.

700 KOPPERS BUILDING-436 SEVENTH AVENUE PHTTSBURGH, PA 15219

20872 Mornison & Foerster LUP 425 Market Street San Francisco, CA 94105 FILING RECEIPT

OC00000011010291

Date Mailed: 10/09/2003

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

Gang Zhang, Pittsburgh, PA; Enis Aykut Dengi, Tempe, AZ; Ronald A. Rohrer, Saratoga, CA;

Assignment For Published Patent Application

Neolinear, Inc.;

Domestic Priority data as claimed by applicant

This appln claims benefit of 60/395,156 07/11/2002

Foreign Applications

If Required, Foreign Filing License Granted: 10/08/2003

Projected Publication Date: 01/15/2004

Non-Publication Request: No

Early Publication Request: No

** SMALL ENTITY **

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WEBB, ZIECTIA REPAREMENTAL LOCISTION
OF THE REPAREMENT AND STATE OF THE PEREMENT AND ST

Title

Analog integrated circuit layout design

Preliminary Class

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